What is claimed is:

1. A method of operating a memory device, comprising:
communicating between the memory device and a logic device separate from the memory device, wherein communicating occurs across a local bus at voltage levels compatible with internal logic levels of the memory device.

2. The method of claim 1, further comprising:
communicating between the logic device and a system bus, wherein the system bus is distinct and isolated from the local bus.

3. The method of claim 1, wherein communications across the local bus to the memory device are received by at least one nominally-buffered signal line of the memory device.

4. The method of claim 3, wherein the at least one nominally-buffered signal line includes a non-buffered signal line.

5. The method of claim 1, further comprising:
sending a decoded address signal from the logic device to the memory device; and
accessing a memory array of the memory device in response to the decoded address signal without further address decoding.

6. The method of claim 1, further comprising:
sending a decoded command signal from the logic device to the memory device; and
controlling operations on a memory array of the memory device in response to the decoded command signal without further command interpretation.

7. A method of operating an electronic system having a memory device and a logic device separate from the memory device, the method comprising:

communicating between the memory device and the logic device across a local bus at voltage levels compatible with internal logic levels of the memory device, wherein the local bus comprises a plurality of direct connections between the memory device and the logic device; and

communicating between the logic device and a system bus, wherein the system bus is distinct and isolated from the local bus.

8. The method of claim 7, wherein communications across the local bus to the memory device are received by at least one nominally-buffered signal line of the memory device.

9. The method of claim 8, wherein the at least one nominally-buffered signal line includes a non-buffered signal line.

10. The method of claim 7, wherein voltage levels for communication across the system bus are higher than the internal logic levels of the memory device.

11. The method of claim 7, wherein the system bus has a length that is at least an order of magnitude greater than a length of the local bus.

12. The method of claim 7, wherein the system bus has a bit width that is less than a bit width of the local bus.

13. The method of claim 7, wherein communicating between the memory device and the logic device across the local bus occurs at a first frequency and communicating between the logic device and the system bus occurs at a second frequency, wherein the first frequency is higher than the second frequency.

14. The method of claim 7, wherein communicating between the memory device and the logic device across the local bus occurs at a first word size and communicating between the logic device and the system bus occurs at a second word size, wherein the first word size is larger than the second word size.

15. The method of claim 7, further comprising:
sending a decoded address signal from the logic device to the memory device; and
accessing a memory array of the memory device in response to the decoded address signal without further address decoding.

16. The method of claim 7, further comprising:
sending a decoded command signal from the logic device to the memory device; and
controlling operations on a memory array of the memory device in response to the decoded command signal without further command interpretation.

17. A method of operating an electronic system having a memory device and a logic device separate from the memory device, the method comprising:
communicating between the memory device and the logic device across a local bus at voltage levels compatible with internal logic levels of the memory device; and
communicating between the logic device and a system bus;
wherein voltage levels for communication across the system bus are higher than the internal logic levels of the memory device;
wherein the local bus comprises a plurality of direct connections between the memory device and the logic device; and
wherein the system bus is distinct and isolated from the local bus and has a bit width that is less than a bit width of the local bus.

18. The method of claim 17, wherein the system bus has a length that is at least an order of magnitude greater than a length of the local bus.

19. The method of claim 17, wherein communicating between the memory device and the logic device across the local bus occurs at a first frequency and communicating between the logic device and the system bus occurs at a second frequency, wherein the first frequency is higher than the second frequency.

20. The method of claim 17, wherein communicating between the memory device and the logic device across the local bus occurs at a first word size and communicating between the logic device and the system bus occurs at a second word size, wherein the first word size is larger than the second word size.

21. The method of claim 17, further comprising:
sending a decoded address signal from the logic device to the memory device; and
accessing a memory array of the memory device in response to the decoded address signal without further address decoding.

22. The method of claim 17, further comprising:
sending a decoded command signal from the logic device to the memory device; and
controlling operations on a memory array of the memory device in response to the decoded command signal without further command interpretation.

23. A method of operating an electronic system having a memory device and a logic device separate from the memory device, the method comprising:
communicating between the memory device and the logic device across a local bus at voltage levels compatible with internal logic levels of the memory device; and

communicating between the logic device and a system bus at voltage levels higher than the internal logic levels of the memory device;

wherein the local bus comprises a plurality of direct connections between the memory device and the logic device; and

wherein the system bus is distinct and isolated from the local bus and has a length that is at least an order of magnitude greater than a length of the local bus.

24. The method of claim 23, wherein the system bus has a bit width that is less than a bit width of the local bus.

25. The method of claim 23, wherein communicating between the memory device and the logic device across the local bus occurs at a first frequency and communicating between the logic device and the system bus occurs at a second frequency, wherein the first frequency is higher than the second frequency.

26. The method of claim 23, wherein communicating between the memory device and the logic device across the local bus occurs at a first word size and communicating between the logic device and the system bus occurs at a second word size, wherein the first word size is larger than the second word size.

27. The method of claim 23, further comprising:

sending a decoded address signal from the logic device to the memory device; and

accessing a memory array of the memory device in response to the decoded address signal without further address decoding.

28. The method of claim 23, further comprising:

sending a decoded command signal from the logic device to the memory device; and

controlling operations on a memory array of the memory device in response to the decoded command signal without further command interpretation.

29. A method of operating an electronic system having a memory device and a logic device separate from the memory device, the method comprising:

communicating between the memory device and the logic device across a local bus, wherein the local bus comprises a plurality of direct connections between the memory device and the logic device and wherein the local bus is distinct and isolated from a system bus; and

communicating between the logic device and the system bus, wherein the system bus has a bit width that is less than a bit width of the local bus.

30. The method of claim 29, wherein communicating with the memory device occurs only through the logic device and the local bus.

31. A method of operating an electronic system having a memory device and a logic device separate from the memory device, the method comprising:

communicating between the memory device and the logic device at a first frequency across a local bus; and

communicating between the logic device and a system bus at a second frequency lower than the first frequency;

wherein the local bus comprises a plurality of direct connections between the memory device and the logic device;

wherein the system bus is distinct and isolated from the local bus and has a length that is at least an order of magnitude greater than a length of the local bus; and

wherein the system bus has a bit width that is less than a bit width of the local bus.

32. The method of claim 31, wherein communicating between the memory device and the logic device across the local bus occurs at a first word size and communicating between the logic device and the system bus occurs at a second word size, wherein the first word size is larger than the second word size.

33. The method of claim 31, further comprising:
sending a decoded address signal from the logic device to the memory device; and
accessing a memory array of the memory device in response to the decoded address signal without further address decoding.

34. The method of claim 31, further comprising:
sending a decoded command signal from the logic device to the memory device; and
controlling operations on a memory array of the memory device in response to the decoded command signal without further command interpretation.

35. A memory device, comprising:
a memory array; and
at least one nominally-buffered signal line, substantially incapable of level translation, for communication between the memory array and an external device.

36. The memory device of claim 35, wherein the at least one nominally-buffered signal line is a data signal line.

37. The memory device of claim 35, wherein the at least one nominally-buffered signal line is an address signal line.

38. The memory device of claim 35, wherein the at least one nominally-buffered signal line is a control signal line.

39. The memory device of claim 35, wherein each signal line for communication between the memory device and the external device is a nominally-buffered signal line.

40. The memory device of claim 35, wherein the at least one nominally-buffered signal line is a non-buffered signal line.

41. The memory device of claim 35, wherein the memory array is an array of non-volatile floating-gate memory cells and wherein the external device is a logic device.

42. The memory device of claim 35, wherein the at least one nominally-buffered signal line is multiplexed to service more than one signal.

43. The memory device of claim 35, wherein the at least one nominally-buffered signal line comprises:
a plurality of nominally-buffered data signal lines;
a plurality of nominally-buffered address signal lines; and
a plurality of nominally-buffered control signal lines.

44. The memory device of claim 35, wherein the at least one nominally-buffered signal line comprises:
at least one control signal line for receiving control signals from the external device;
at least one address signal line for receiving address signals from the external device for accessing a portion of the memory array in response to the control signals; and
at least one data signal line for receiving data signals from the external device for writing to the accessed portion of the memory array.

45. The memory device of claim 35, wherein the memory device is devoid of logic functions capable of command interpretation.

46. The memory device of claim 35, wherein the memory device is devoid of logic functions capable of address decoding.

47. A memory device, comprising:
a memory array; and
at least one control signal line for receiving decoded control signals from the external device to control operations on the memory array;
wherein the memory device is devoid of logic functions capable of command interpretation.

48. The memory device of claim 47, wherein each control signal line is a nominally-buffered signal line.

49. The memory device of claim 47, wherein the at least one control signal line is a non-buffered signal line.

50. The memory device of claim 47, wherein the memory array is an array of non-volatile floating-gate memory cells and wherein the external device is a logic device.

51. A memory device, comprising:
a memory array;
at least one address signal line for receiving decoded address signals from the external device; and
access circuitry to provide access to the memory array in response to the decoded address signals;

wherein the memory device is devoid of logic functions capable of address decoding.

52. The memory device of claim 51, wherein each address signal line is a nominally-buffered signal line.

53. The memory device of claim 51, wherein the at least one address signal line is a non-buffered signal line.

54. The memory device of claim 51, wherein the memory array is an array of non-volatile floating-gate memory cells and wherein the external device is a logic device.

55. A memory device, comprising:

a memory array;

at least one nominally-buffered control signal line, substantially incapable of level translation, for receiving control signals from the external device;

at least one nominally-buffered address signal line, substantially incapable of level translation, for receiving address signals from the external device for accessing a portion of the memory array in response to the control signals; and

at least one nominally-buffered data signal line, substantially incapable of level translation, for communicating data signals between the external device and an accessed portion of the memory array.

56. The memory device of claim 55, wherein each signal line for communication between the memory device and the external device is a nominally-buffered signal line.

57. The memory device of claim 55, wherein at least one nominally-buffered signal line is a non-buffered signal line.

58. The memory device of claim 55, wherein the memory array is an array of non-volatile floating-gate memory cells and wherein the external device is a logic device.

59. The memory device of claim 55, wherein at least one nominally-buffered signal line is multiplexed to service more than one signal.

60. The memory device of claim 55, wherein the memory device is devoid of logic functions capable of command interpretation.

61. The memory device of claim 55, wherein the memory device is devoid of logic functions capable of address decoding.

62. A memory device, comprising:
a memory array;
at least one control signal line for receiving control signals from the external device;
at least one address signal line for receiving address signals from the external device for accessing a portion of the memory array in response to the control signals; and
at least one data signal line for communicating data signals between the external device and an accessed portion of the memory array;
wherein at least one control signal line, address signal line or data signal line is substantially incapable of level translation.

63. The memory device of claim 62, wherein each control signal line, address signal line and data signal line is substantially incapable of level translation.

64. The memory device of claim 62, wherein the memory device is devoid of logic functions capable of command interpretation.

65. The memory device of claim 62, wherein the memory device is devoid of logic functions capable of address decoding.

66. A memory device, comprising:
a memory array;
at least one control signal line for receiving control signals from the external device;
at least one address signal line for receiving address signals from the external device for accessing a portion of the memory array in response to the control signals; and
at least one data signal line for communicating data signals between the external device and an accessed portion of the memory array;
wherein at least one control signal line, address signal line or data signal line is adapted for use with voltage levels that are compatible with internal logic levels of the memory array.

67. An electronic system, comprising:
a logic device for coupling to a system bus;
a memory device separate from the logic device; and
a local bus coupled between the logic device and the memory device;
wherein the memory device includes at least one nominally-buffered signal line coupled to the local bus.

68. The electronic system of claim 67, wherein the at least one nominally-buffered signal line is a non-buffered signal line.

69. The electronic system of claim 67, further comprising:

a plurality of coupling areas on the logic device, including a first portion of the plurality of coupling areas on the logic device for coupling to the system bus and a second portion of the plurality of coupling areas on the logic device for coupling to the local bus;

a plurality of coupling areas on the memory device for coupling to the local bus; and

a plurality of direct connections coupled between the second portion of the plurality of coupling areas on the logic device and the plurality of coupling areas on the memory device, wherein the plurality of direct connections collectively make up the local bus.

70. The electronic system of claim 69, wherein the plurality of direct connections comprises a plurality of wire bond connections.

71. The electronic system of claim 69, wherein the plurality of direct connections comprises a plurality of solder bump connections.

72. The electronic system of claim 69, wherein the plurality of direct connections each have a length of less than about 2mm.

73. The electronic system of claim 69, wherein the plurality of direct connections each have a length of less than about 1mm.

74. The electronic system of claim 67, wherein the at least one nominally-buffered signal line is a data signal line.

75. The electronic system of claim 67, wherein the at least one nominally-buffered signal line is an address signal line.

76. The electronic system of claim 67, wherein the at least one nominally-buffered signal line is a control signal line.

77. The electronic system of claim 67, wherein each signal line for communication between the memory device and the logic device is a nominally-buffered signal line.

78. The electronic system of claim 67, wherein the memory device includes a memory array containing an array of non-volatile floating-gate memory cells.

79. The electronic system of claim 67, wherein the at least one nominally-buffered signal line comprises:
a plurality of nominally-buffered data signal lines;
a plurality of nominally-buffered address signal lines; and
a plurality of nominally-buffered control signal lines.

80. The electronic system of claim 67, wherein the memory device includes a memory array and the at least one nominally-buffered signal line comprises:
at least one control signal line for receiving control signals from the logic device;
at least one address signal line for receiving address signals from the logic device for accessing a portion of the memory array in response to the control signals; and
at least one data signal line for receiving data signals from the logic device for writing to the accessed portion of the memory array.

81. The electronic system of claim 67, wherein the electronic system is a wireless communication device.

82. The electronic system of claim 67, wherein the memory device is devoid of logic functions capable of command interpretation.

83. The electronic system of claim 67, wherein the memory device is devoid of logic functions capable of address decoding.

84. An electronic system, comprising:
a logic device for coupling to a system bus;
a memory device separate from the logic device; and
a local bus coupled between the logic device and the memory device;
wherein the memory device includes at least one nominally-buffered signal line coupled to the local bus; and
wherein the memory device is devoid of logic functions capable of address decoding.

85. The electronic system of claim 84, wherein the memory device is further devoid of logic functions capable of command interpretation.

86. An electronic system, comprising:
a logic device for coupling to a system bus;
a memory device separate from the logic device; and
a local bus coupled between the logic device and the memory device;
wherein the memory device includes at least one nominally-buffered signal line coupled to the local bus; and
wherein the memory device is devoid of logic functions capable of command interpretation.